ABSTRACT

A digital embedded architecture, includes a microcontroller and a memory device, suitable for reconfigurable computing in digital signal processing and comprising: a processor, structured to implement a Very Long Instruction Word elaboration mode by a general purpose hardwired computational logic, and an additional data elaboration channel comprising a reconfigurable function unit based on a pipelined array of configurable look-up table based cells controlled by a special purpose control unit, thus easing the elaboration of critical kernels algorithms.